PAN	ĴΪΤ
	SEMI CONDUCTOR

PJQ5476AL

100V N-Channel Enhancement Mode MOSFET

Voltage

Current 42A

Features

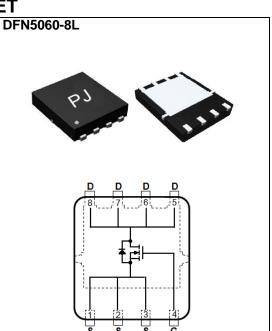
- RDS(ON) , VGS@10V, ID@20A<25m Ω
- RDS(ON) , VGS@4.5V, ID@15A<28.5mΩ

100 V

- Advanced Trench Process Technology
- High density cell design for ultra low on-resistance
- Lead free in compliance with EU RoHS 2011/65/EU directive
- Green molding compound as per IEC61249 Std. (Halogen Free)

Mechanical Data

- Case: DFN5060-8L Package
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.0028 ounces, 0.08 grams
- Marking: Q5476AL



Maximum Ratings and Thermal Characteristics ($T_A=25^{\circ}C$ unless otherwise noted)

PARAME	TER	SYMBOL	LIMIT	UNITS	
Drain-Source Voltage		V _{DS}	100	V	
Gate-Source Voltage		V_{GS}	<u>+</u> 20	V	
Continuous Drain Current	T _C =25°C		42		
	T _C =100°C	ID	26.6	А	
Pulsed Drain Current (Note 1)	T _C =25°C	I _{DM}	150		
Power Dissipation	T _C =25°C	6	83	14/	
	$T_{\rm C}=100^{\circ}{\rm C}$	Po	33	W	
Continuous Drain Current	T _A =25°C		6.5	А	
	T _A =70°C	I _D	5.2	А	
Power Dissipation	T _A =25°C	6	2.0		
	T _A =70°C	Po	1.3	W	
Single Pulse Avalanche Energy ^(Note 6)		E _{AS}	63.4	mJ	
Operating Junction and Storage Temperature Range		T _J ,T _{STG}	-55~150	°C	
Typical Thermal Resistance ^(Note 4,5)	Junction to Case	R _{θJC}	1.5	00000	
	Junction to Ambient	R _{θJA}	62.5	°C/W	



Electrical Characteristics ($T_A=25^{\circ}C$ unless otherwise noted)

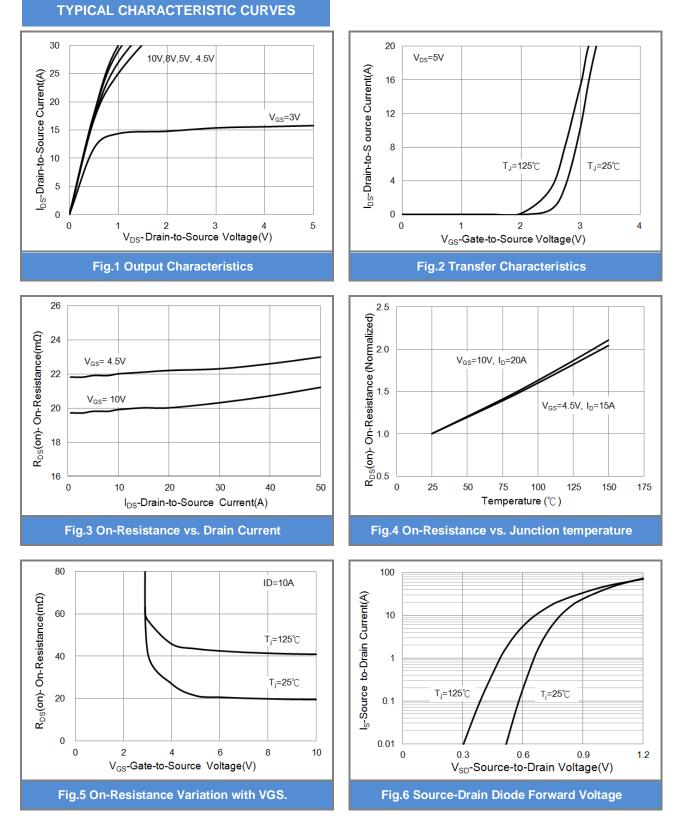
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	V _{GS} =0V,I _D =250uA	100	-	-	V
Gate Threshold Voltage	V _{GS(th)}	$V_{DS}=V_{GS}$, $I_{D}=250$ uA	1.0	1.8	2.5	V
Drain-Source On-State Resistance	ſ	V _{GS} =10V,I _D =20A	-	20	25	mΩ
	R _{DS(on)}	V _{GS} =4.5V,I _D =15A	-	22	28.5	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =80V,V _{GS} =0V	-	-	1.0	uA
Gate-Source Leakage Current	I _{GSS}	V _{GS} = <u>+</u> 20V,V _{DS} =0V	-	-	<u>+</u> 100	nA
Dynamic (Note 7)						
Total Gate Charge	Qg	V _{DS} =50V, I _D =10A, V _{GS} =10V ^(Note 1,2)	-	31	-	nC
Gate-Source Charge	Q _{gs}		-	5.1	-	
Gate-Drain Charge	Q _{gd}		-	7.3	-	
Input Capacitance	Ciss	V _{DS} =30V, V _{GS} =0V, f=1.0MHZ	-	1519	-	pF
Output Capacitance	Coss		-	132	-	
Reverse Transfer Capacitance	Crss		-	66	-	
Turn-On Delay Time	td _(on)	V_{DD} =50V, I_{D} =10A, V_{GS} =10V, R_{G} =3 Ω ^(Note 1,2)	-	11	-	
Turn-On Rise Time	t _r		-	42	-	ns
Turn-Off Delay Time	td _(off)		-	40	-	
Turn-Off Fall Time	t _f	$R_{G}=3\Omega$	-	19	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I _S		-	-	42	А
Diode Forward Voltage	V _{SD}	I _S =1A,V _{GS} =0V	-	0.7	1.2	V

NOTES :

- 1. Pulse width</br>
- 2. Essentially independent of operating temperature typical characteristics.
- 3. Repetitive rating, pulse width limited by junction temperature TJ(MAX)=150°C. Ratings are based on low frequency and duty cycles to keep initial TJ =25°C.
- 4. The maximum current rating is package limited.
- 5. $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch² with 2oz.square pad of copper.
- 6. The test condition is L=3mH, $I_{\text{AS}}{=}6.5\text{A},\,V_{\text{DD}}{=}50\text{V},\,V_{\text{GS}}{=}10\text{V}$
- 7. Guaranteed by design, not subject to production testing.

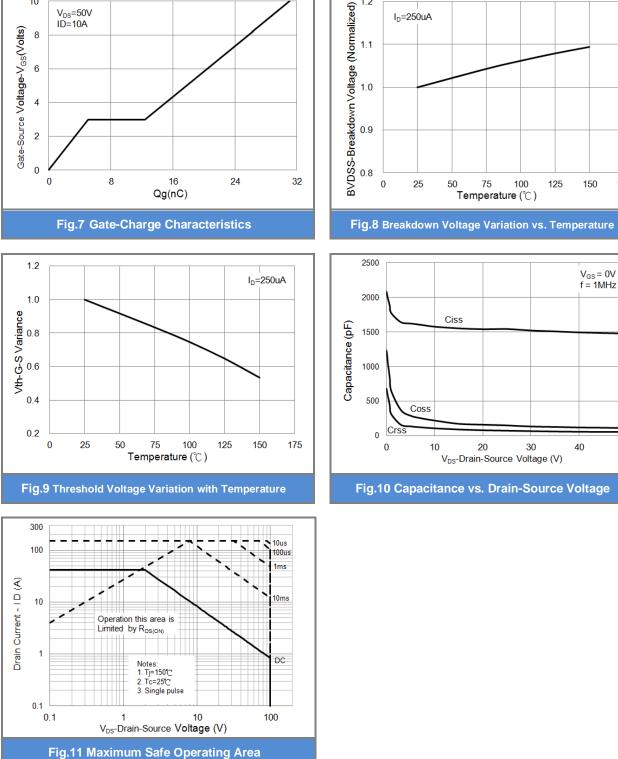
January 14,2016-REV.01

Page 3





PJQ5476AL



1.2

I_D=250uA



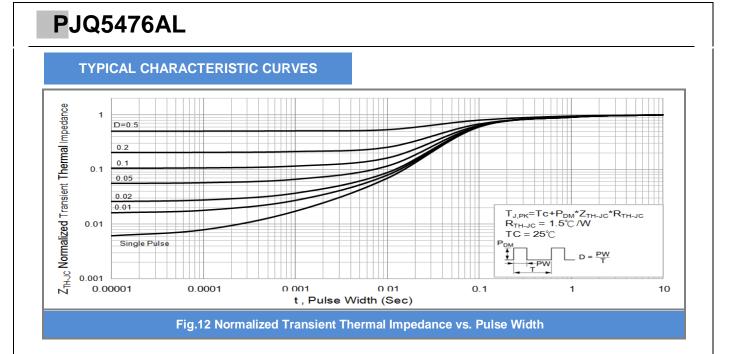
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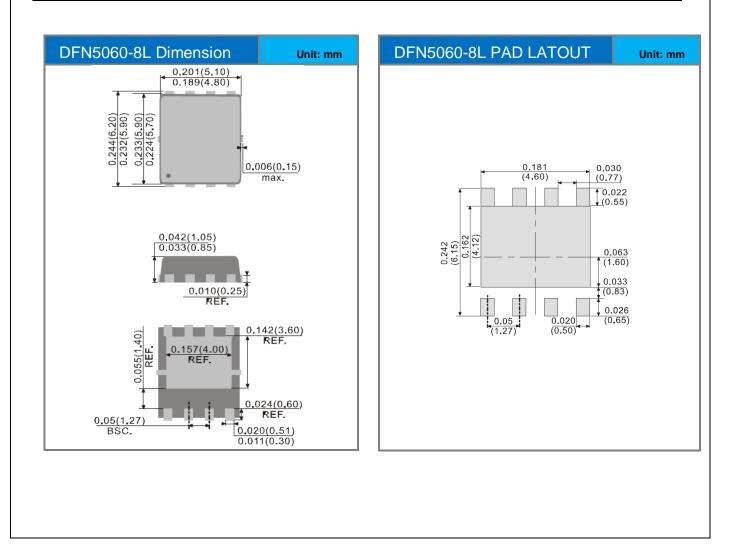


PJQ5476AL

PART NO PACKING CODE VERSION

Part No Packing Code	Package Type	Packing type	Marking	Version
PJQ5476AL_R2_00001	DFN5060-8L	3000pcs / 13" reel	Q5476AL	Halogen free

Packaging Information & Mounting Pad Layout





PJQ5476AL

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