PJL9801

30V P-Channel Enhancement Mode MOSFET

Voltage	-30 V	Current	-5A

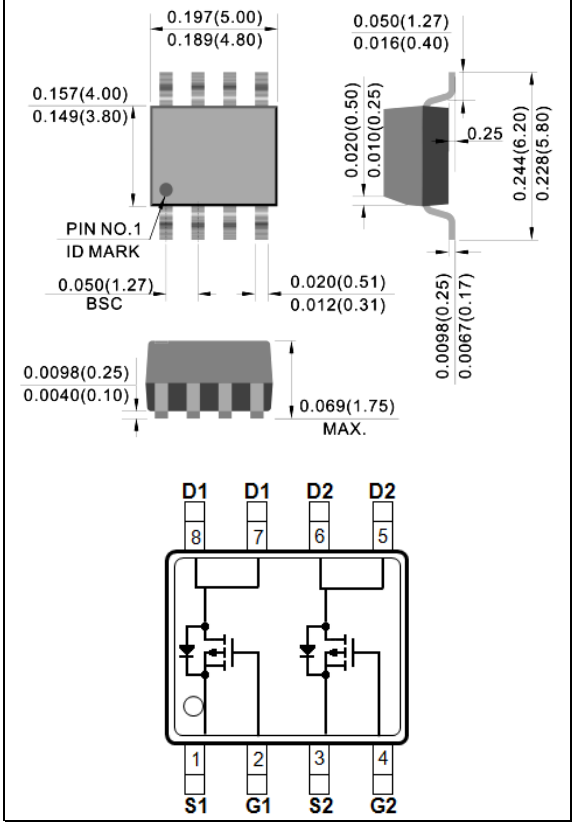
Features

- RDS(ON) , VGS@-10V, ID@-5.0A<54mΩ
- RDS(ON) , VGS@-4.5V, ID@-3.5A<61mΩ
- RDS(ON) , VGS@-2.5V, ID@-2.5A<82mΩ
- Advanced Trench Process Technology
- High density cell design for ultra low on-resistance
- Lead free in compliance with EU RoHS 2011/65/EU directive
- Green molding compound as per IEC61249 Std. (Halogen Free)

Mechanical Data

- Case: SOP-8 Package
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.0029 ounces, 0.083 grams
- Marking: L9801

SOP-8 **Unit: inch(mm)**



Maximum Ratings and Thermal Characteristics (T_A=25°C unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current		I_D	5	A
Pulsed Drain Current		I_{DM}	20	A
Power Dissipation	T_a=25°C	P_D	2	W
	Derate above 25°C		16	mW/°C
Operating Junction and Storage Temperature Range		T_J,T_{STG}	-55~150	°C
Typical Thermal resistance - Junction to Ambient (Note 3)		$R_{\theta JA}$	62.5	°C/W

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Electrical Characteristics (T_A=25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V,I_D=-250uA	-30	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=-250uA	-0.5	-0.97	-1.3	V
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS}=-10V,I_D=-5.0A	-	45	54	mΩ
		V_{GS}=-4.5V,I_D=-3.5A	-	51	61	
		V_{GS}=-2.5V,I_D=-2.5A	-	67	82	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-30V,V_{GS}=0V	-	-0.01	-1.0	uA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±12V,V_{DS}=0V	-	±10	±100	nA
Dynamic(Note 5)						
Total Gate Charge	Q_g	V_{DS}=-15V, I_D=-5.0A, V_{GS}=4.5V (Note 1,2)	-	9.1	-	nC
Gate-Source Charge	Q_{gs}		-	1.8	-	
Gate-Drain Charge	Q_{gd}		-	2.6	-	
Input Capacitance	Ciss	V_{DS}=-15V, V_{GS}=0V, f=1.0MHZ	-	816	-	pF
Output Capacitance	Coss		-	64	-	
Reverse Transfer Capacitance	Crss		-	42	-	
Turn-On Delay Time	$td_{(on)}$	V_{DD}=-15V, I_D=-5.0A, V_{GS}=-10V, R_G=6Ω (Note 1,2)	-	5	-	ns
Turn-On Rise Time	tr		-	45	-	
Turn-Off Delay Time	$td_{(off)}$		-	66	-	
Turn-Off Fall Time	tf		-	10	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I_S	---	-	-	-2	A
Diode Forward Voltage	V_{SD}	I_S=-1.0A, V_{GS}=0V	-	0.77	-1.2	V

NOTES :

1. Pulse width≤300us, Duty cycle≤2%
2. Essentially independent of operating temperature typical characteristics.
3. The maximum current rating is package limited.
4. $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 $inch^2$ with 2oz.square pad of copper
5. Guaranteed by design, not subject to production testing

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TYPICAL CHARACTERISTIC CURVES

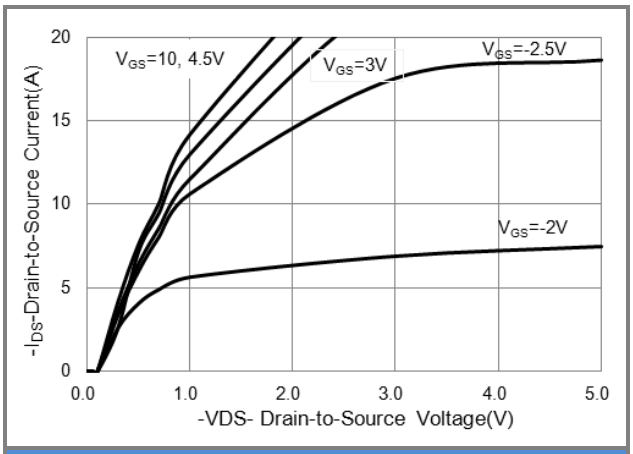

Fig.1 On-Region Characteristics

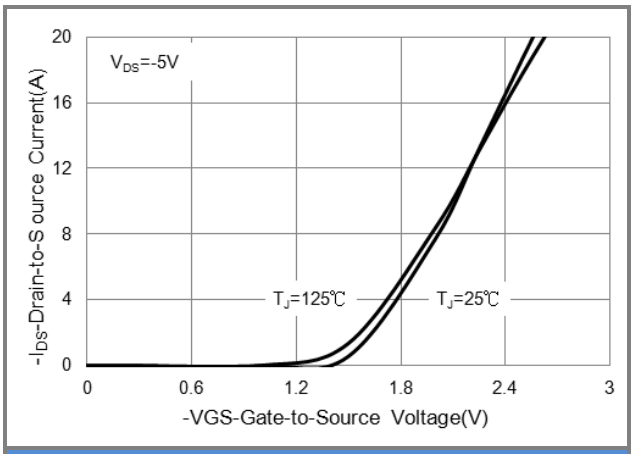

Fig.2 Transfer Characteristics

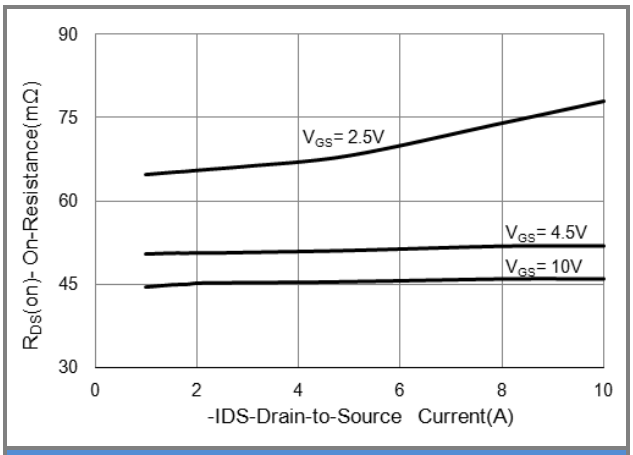

Fig.3 On-Resistance vs. Drain Current

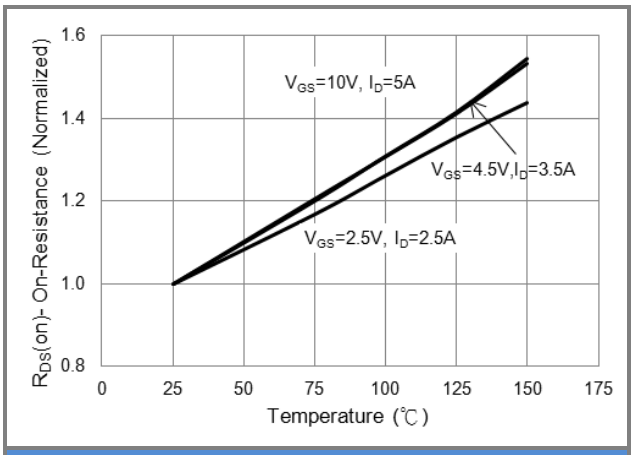

Fig.4 On-Resistance vs. Junction temperature

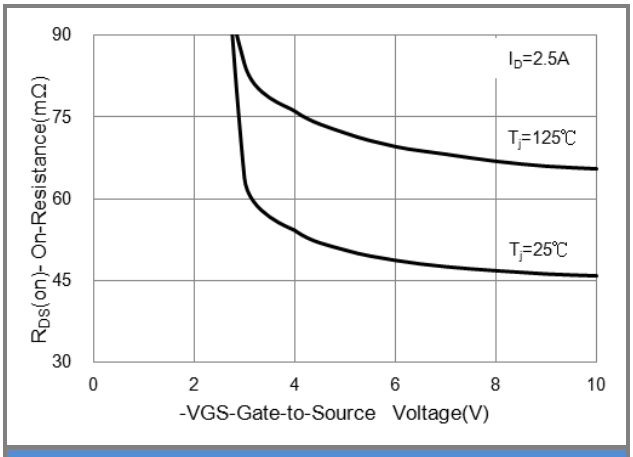

Fig.5 On-Resistance Variation with VGS.

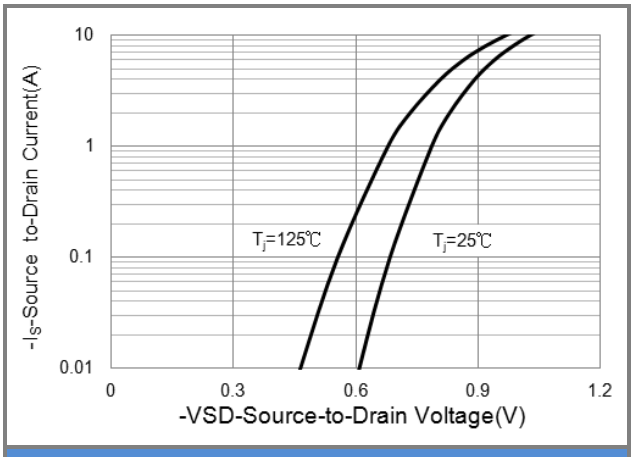

Fig.6 Body Diode Characteristics

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TYPICAL CHARACTERISTIC CURVES

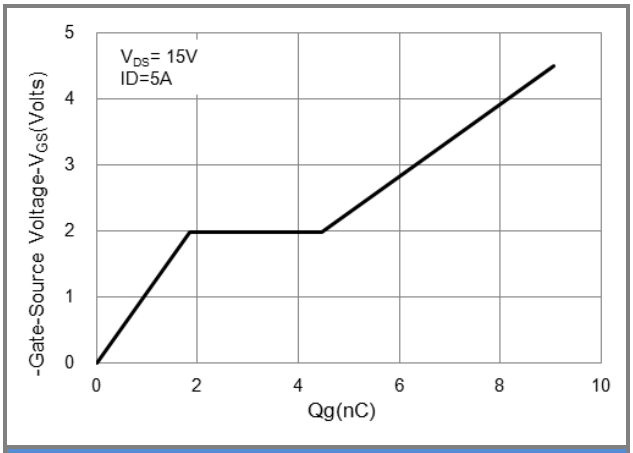

Fig.7 Gate-Charge Characteristics

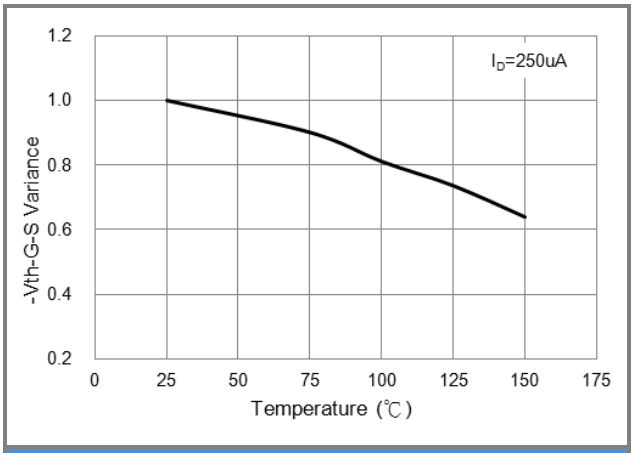

Fig.8 Threshold Voltage Variation with Temperature.

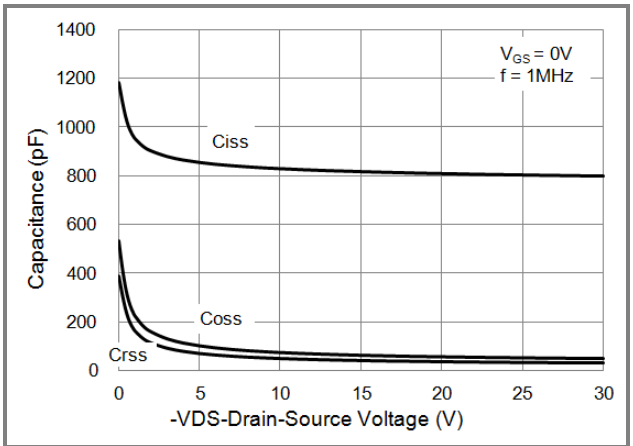

Fig.9 Capacitance vs. Drain-Source Voltage.

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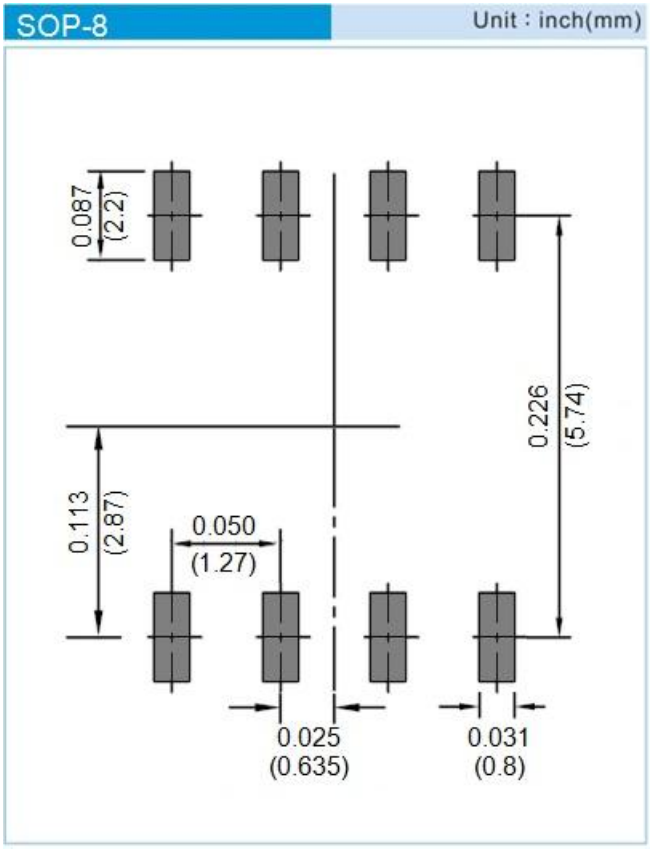
PART NO PACKING CODE VERSION

Part No Packing Code	Package Type	Packing type	Marking	Version
PJL9801_R2_00001	SOP-8	2.5K pcs / 13” reel	L9801	Halogen free

MOUNTING PAD LAYOUT



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