



PJT7413

20V P-Channel Enhancement Mode MOSFET – ESD Protected

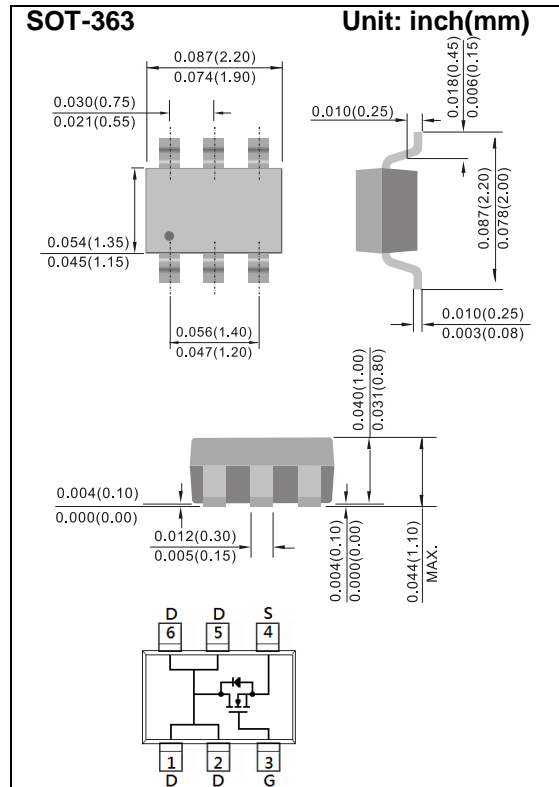
Voltage **-20 V** **Current** **-2.5A**

Features

- RDS(ON) , VGS@-4.5V, ID@-2.5A<85mΩ
- RDS(ON) , VGS@-2.5V, ID@-1.8A<115mΩ
- RDS(ON) , VGS@-1.8V, ID@-1.3A<150mΩ
- RDS(ON) , VGS@-1.5V, ID@-0.5A<250mΩ
- Advanced Trench Process Technology
- Specially Designed for Switch Load, PWM Application, etc.
- Lead free in compliance with EU RoHS 2011/65/EU directive.
- Green molding compound as per IEC61249 Std.
(Halogen Free)

Mechanical Data

- Case: SOT-363 Package
- Terminals: Solderable per MIL-STD-750, Method 2026



Maximum Ratings and Thermal Characteristics (T_A=25°C unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNITS
Drain-Source Voltage	V _{DS}	-20	V
Gate-Source Voltage	V _{GS}	±12	V
Continuous Drain Current	I _D	-2.5	A
Pulsed Drain Current (Note 4)	I _{DM}	-10	A
Power Dissipation	P _D	T _a =25°C	750
		Derate above 25°C	6
Operating Junction and Storage Temperature Range	T _J , T _{STG}	-55~150	°C
Typical Thermal Resistance	R _{θJA}	167	°C/W
- Junction to Ambient (Note 3)			



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Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-20	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.4	-0.65	-1.2	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=-4.5V, I_D=-2.5A$	-	76	85	m Ω
		$V_{GS}=-2.5V, I_D=-1.8A$	-	92	115	
		$V_{GS}=-1.8V, I_D=-1.3A$	-	116	150	
		$V_{GS}=-1.5V, I_D=-0.5A$	-	160	250	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-20V, V_{GS}=0V$	-	-0.01	-1	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 12V, V_{DS}=0V$	-	± 10	± 100	nA
Dynamic (Note 5)						
Total Gate Charge	Q_g	$V_{DS}=-10V, I_D=-2.2A,$ $V_{GS}=-4.5V$ (Note 1,2)	-	7	-	nC
Gate-Source Charge	Q_{gs}		-	1	-	
Gate-Drain Charge	Q_{gd}		-	1.8	-	
Input Capacitance	C_{iss}	$V_{DS}=-10V, V_{GS}=0V,$ $f=1.0\text{MHz}$	-	522	-	pF
Output Capacitance	C_{oss}		-	55	-	
Reverse Transfer Capacitance	C_{rss}		-	40	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD}=-10V, I_D=-2.2A,$ $V_{GS}=-4.5V,$ $R_G=6\Omega$ (Note 1,2)	-	10	-	ns
Turn-On Rise Time	t_r		-	4	-	
Turn-Off Delay Time	$t_{d(off)}$		-	34	-	
Turn-Off Fall Time	t_f		-	5	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I_S	---	-	-	-1.0	A
Diode Forward Voltage	V_{SD}	$I_S=-1.0A, V_{GS}=0V$	-	-0.77	-1.2	V

NOTES :

1. Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$
2. Essentially independent of operating temperature typical characteristics.
3. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins mounted on a 1 inch FR-4 with 2oz. square pad of copper.
4. The maximum current rating is package limited.
5. Guaranteed by design, not subject to production testing



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TYPICAL CHARACTERISTIC CURVES

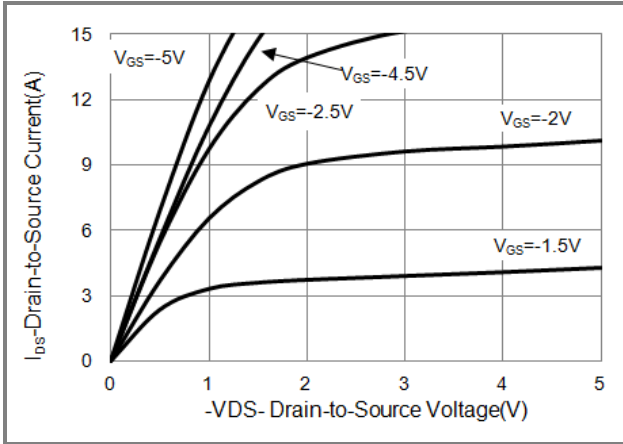


Fig.1 On-Region Characteristics

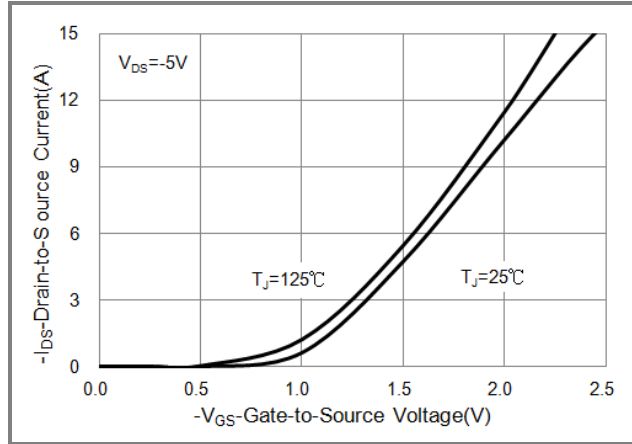


Fig.2 Transfer Characteristics

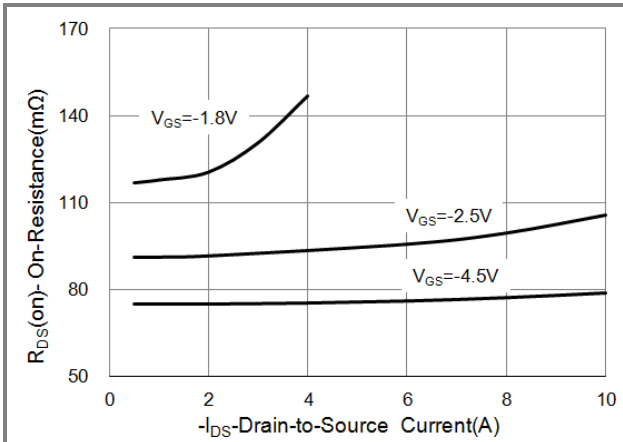


Fig.3 On-Resistance vs. Drain Current

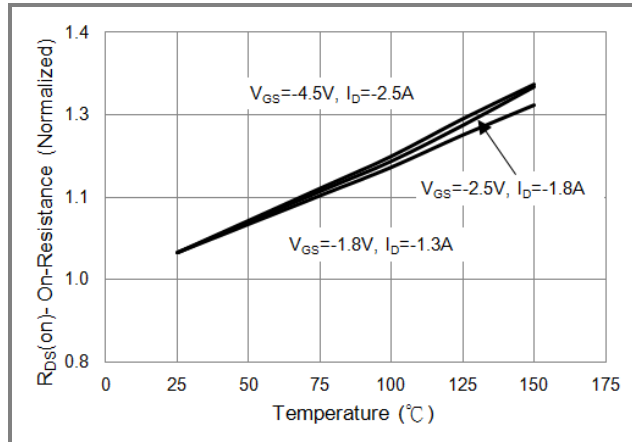


Fig.4 On-Resistance vs. Junction temperature

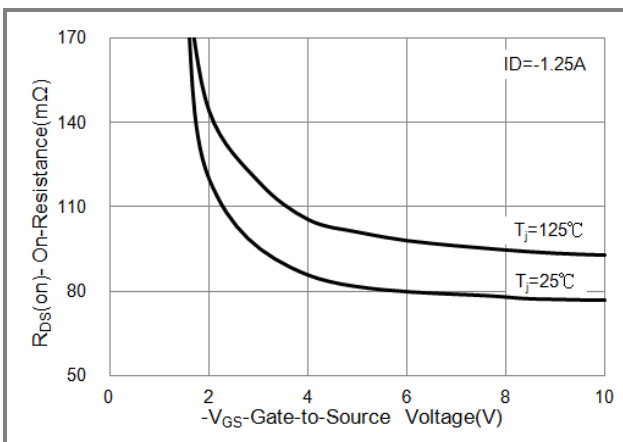


Fig.5 On-Resistance Variation with VGS.

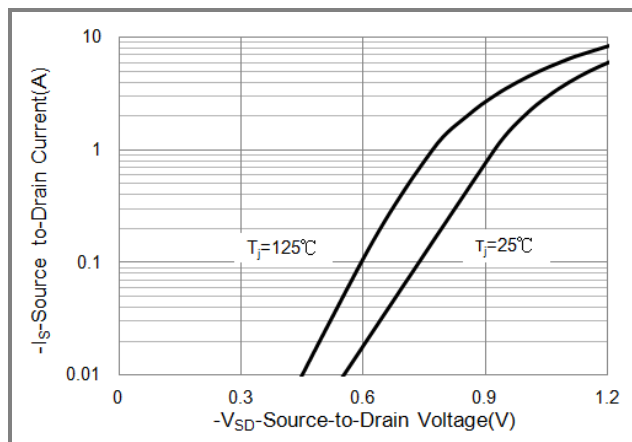


Fig.6 Body Diode Characteristics



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TYPICAL CHARACTERISTIC CURVES

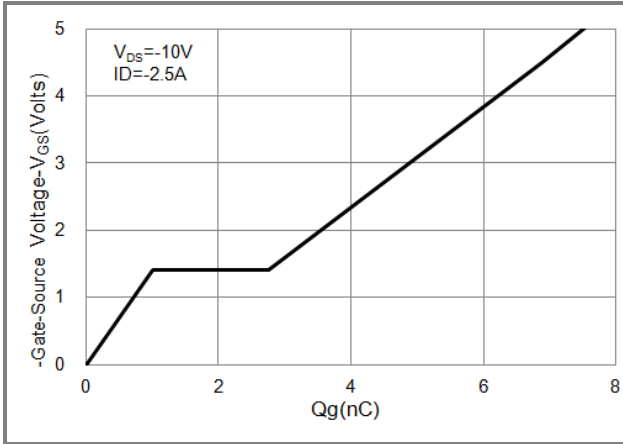


Fig.7 Gate-Charge Characteristics

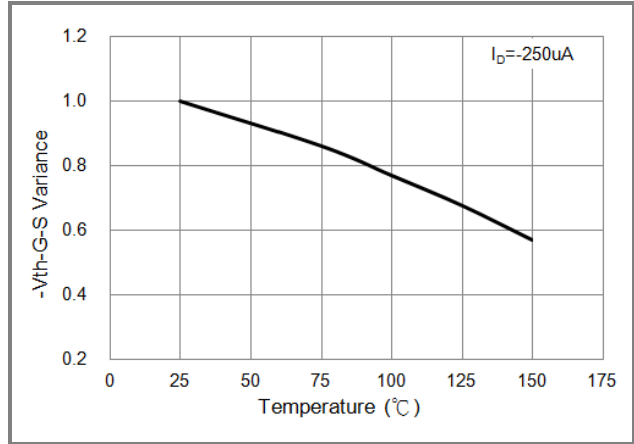


Fig.8 Threshold Voltage Variation with Temperature.

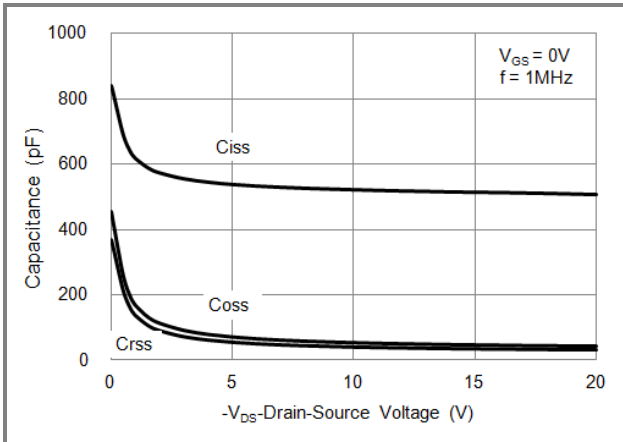


Fig.9 Capacitance vs. Drain-Source Voltage.

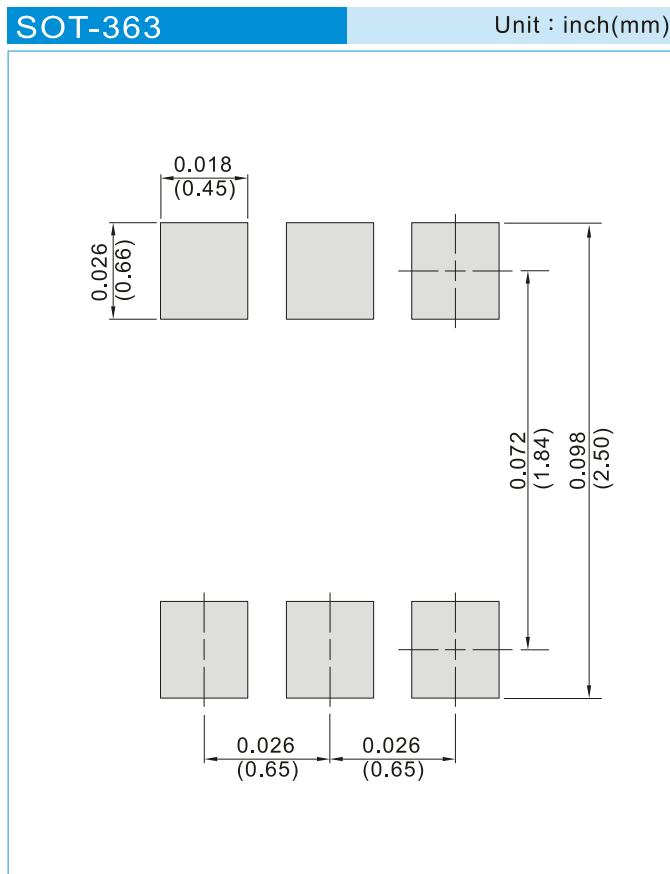


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PART NO PACKING CODE VERSION

Part No Packing Code	Package Type	Packing Type	Marking	Version
PJT7413_S1_00001	SOT-363	3K pcs / 7" reel	T13	Halogen free
PJT7413_S2_00001	SOT-363	10K pcs / 13" reel	T13	Halogen free

MOUNTING PAD LAYOUT





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