



PJS6816

20V N-Channel Enhancement Mode MOSFET

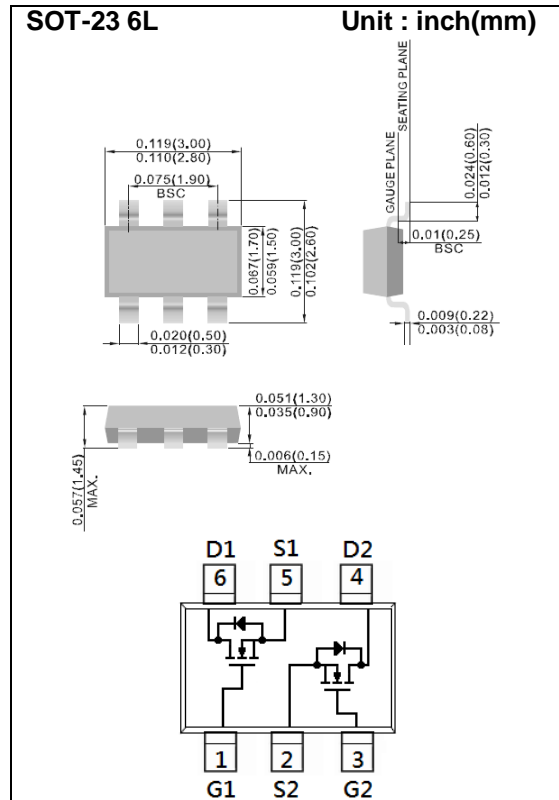
Voltage	20 V	Current	5.2A
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Features

- $R_{DS(ON)}$, $V_{GS}@4.5V$, $I_D@5.2A < 29m\Omega$
- $R_{DS(ON)}$, $V_{GS}@2.5V$, $I_D@3.7A < 42m\Omega$
- $R_{DS(ON)}$, $V_{GS}@1.8V$, $I_D@1.6A < 85m\Omega$
- Advanced Trench Process Technology
- Specially Designed for Switch Load, PWM Application, etc
- Lead free in compliance with EU RoHS 2011/65/EU directive.
- Green molding compound as per IEC61249 Std. (Halogen Free)

Mechanical Data

- Case: SOT-23 6L Package
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.0005 ounces, 0.014 grams
- Marking: S16



Maximum Ratings and Thermal Characteristics ($T_A=25^\circ C$ unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNITS
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 12	V
Continuous Drain Current	I_D	5.2	A
Pulsed Drain Current	I_{DM}	20.8	A
Power Dissipation	P_D	$T_a=25^\circ C$	1.25
		Derate above $25^\circ C$	10
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55~150	$^\circ C$
Typical Thermal resistance	$R_{\theta JA}$	100	$^\circ C/W$
- Junction to Ambient (Note 3)			



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Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	20	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.5	0.77	1.2	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=5.2A$	-	26	29	m Ω
		$V_{GS}=2.5V, I_D=3.7A$	-	35	42	
		$V_{GS}=1.8V, I_D=1.6A$	-	62	85	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=20V, V_{GS}=0V$	-	0.01	1	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 12V, V_{DS}=0V$	-	± 10	± 100	nA
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=10V, I_D=5.2A,$ $V_{GS}=4.5V$ (Note 1,2)	-	7	-	nC
Gate-Source Charge	Q_{gs}		-	1.3	-	
Gate-Drain Charge	Q_{gd}		-	2	-	
Input Capacitance	C_{iss}	$V_{DS}=10V, V_{GS}=0V,$ $f=1.0\text{MHz}$	-	513	-	pF
Output Capacitance	C_{oss}		-	74	-	
Reverse Transfer Capacitance	C_{rss}		-	60	-	
Switching						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD}=10V, I_D=5.2A,$ $V_{GS}=4.5V,$ $R_G=6\Omega$ (Note 1,2)	-	6.2	-	ns
Turn-On Rise Time	t_r		-	56	-	
Turn-Off Delay Time	$t_{d(off)}$		-	23	-	
Turn-Off Fall Time	t_f		-	13	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I_S	---	-	-	1.5	A
Diode Forward Voltage	V_{SD}	$I_S=1.0A, V_{GS}=0V$	-	0.71	1.2	V

NOTES :

1. Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$
2. Essentially independent of operating temperature typical characteristics.
3. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins mounted on a 1 inch FR-4 with 2oz. square pad of copper
4. The maximum current rating is package limited



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TYPICAL CHARACTERISTIC CURVES

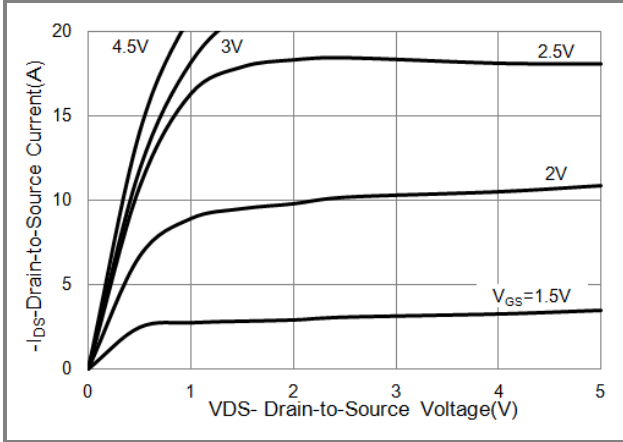


Fig.1 On-Region Characteristics

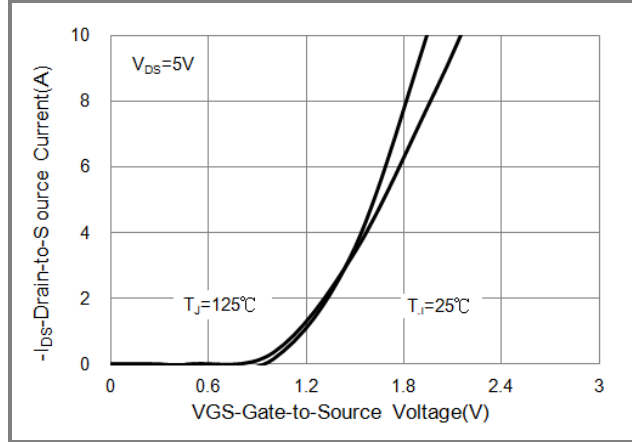


Fig.2 Transfer Characteristics

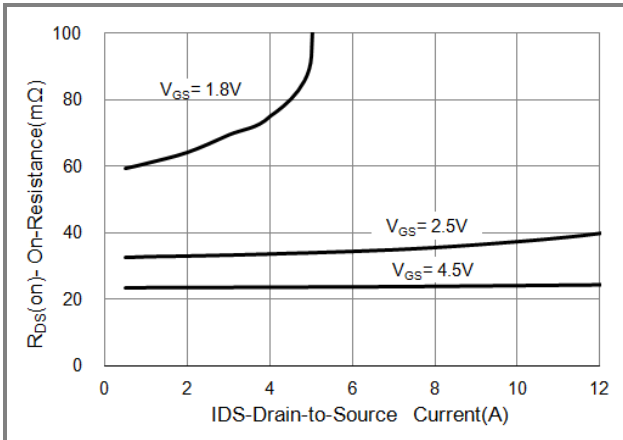


Fig.3 On-Resistance vs. Drain Current

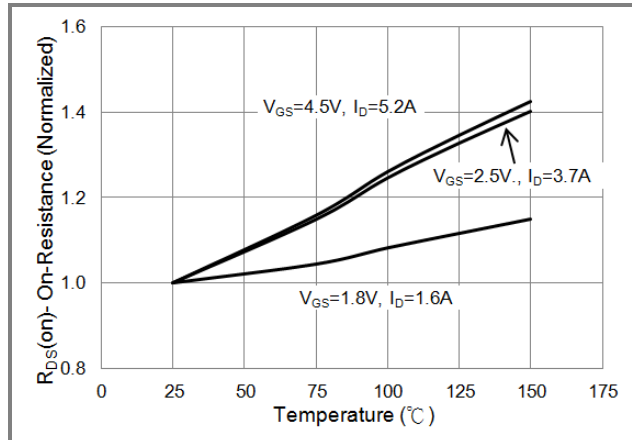


Fig.4 On-Resistance vs. Junction temperature

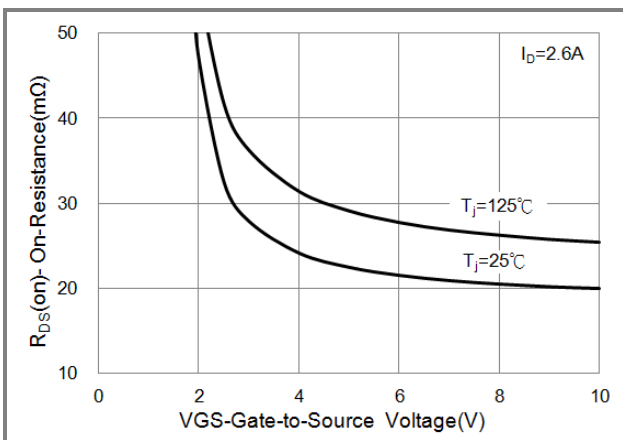


Fig.5 On-Resistance Variation with VGS.

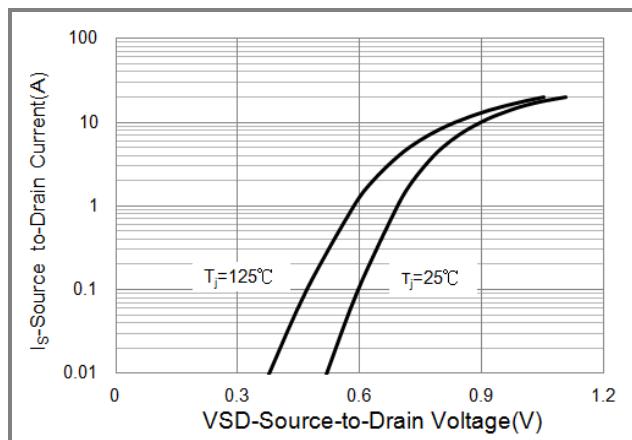


Fig.6 Body Diode Characteristics



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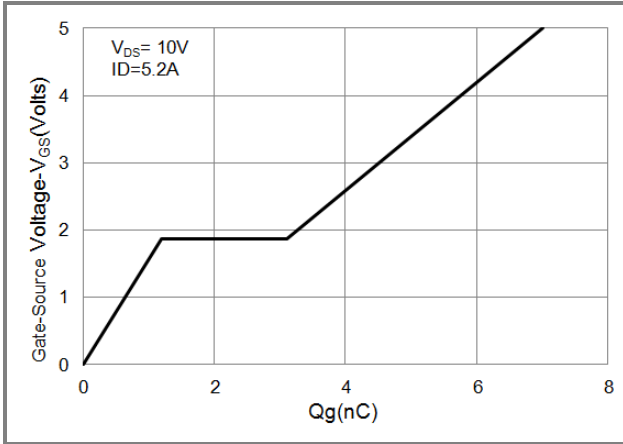


Fig.7 Gate-Charge Characteristics

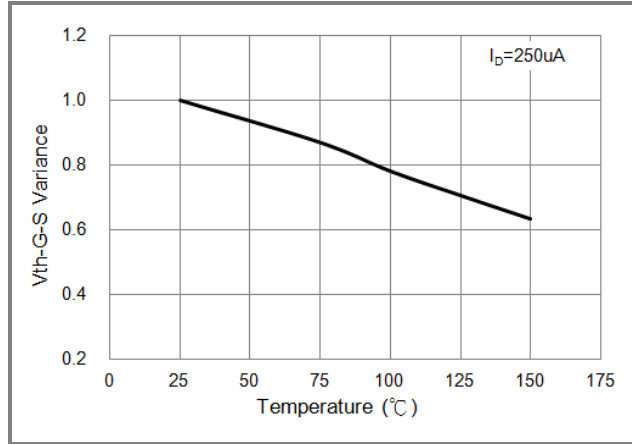


Fig.8 Threshold Voltage Variation with Temperature

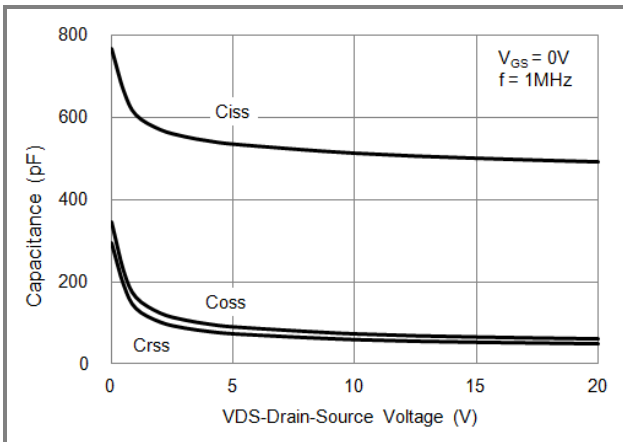


Fig.9 Capacitance vs. Drain-Source Voltage.

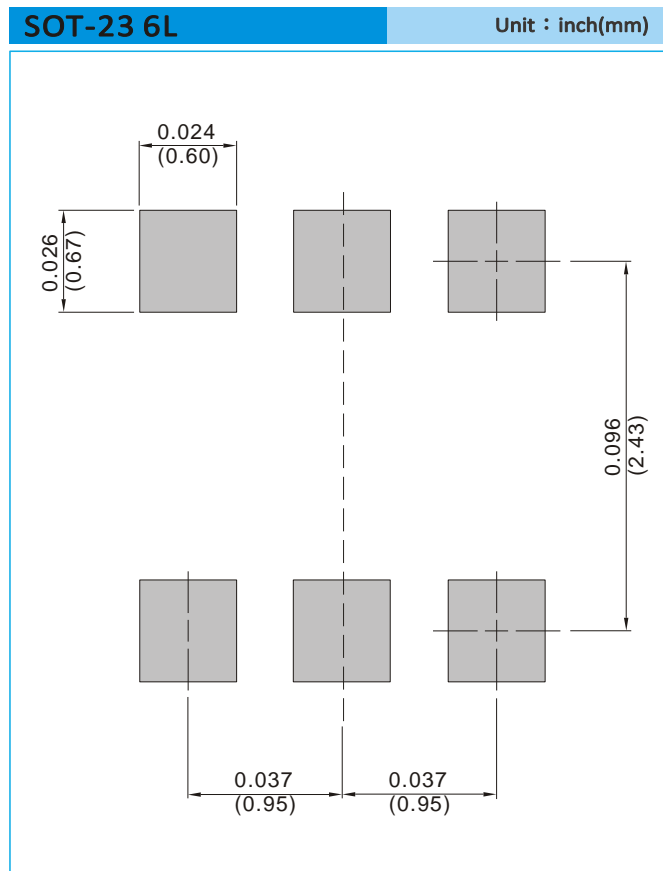


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PART NO PACKING CODE VERSION

Part No Packing Code	Package Type	Packing type	Marking	Version
PJS6816_S1_00001	SOT-23 6L	3K pcs / 7" reel	SE6	Halogen free
PJS6816_S2_00001	SOT-23 6L	10K pcs / 13" reel	SE6	Halogen free

MOUNTING PAD LAYOUT





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