



PJS6604

30V Complementary Enhancement Mode MOSFET

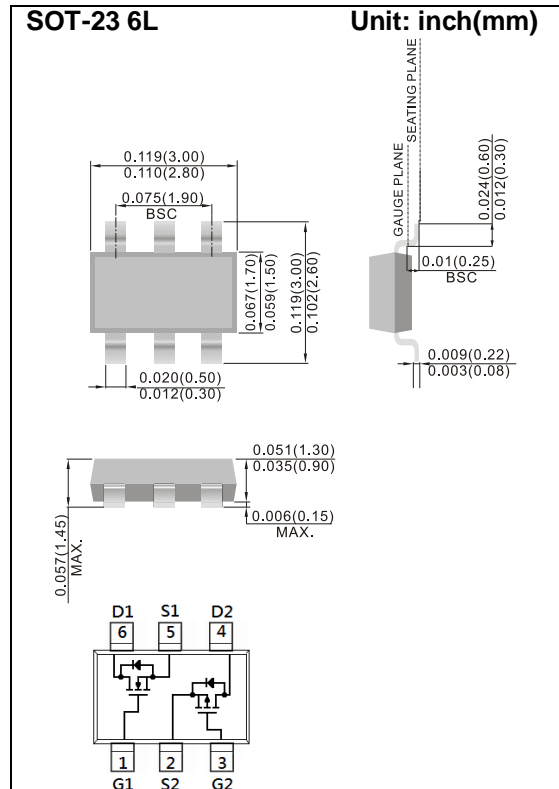
Voltage 30 / -30V **Current** 4.4 / -3.1A

Features

- Advanced Trench Process Technology
- Specially Designed for Switch Load, PWM Application, etc.
- Lead free in compliance with EU RoHS 2011/65/EU directive
- Green molding compound as per IEC61249 Std. (Halogen Free)

Mechanical Data

- Case: SOT-23 6L Package
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.0005 ounces, 0.014 grams



Maximum Ratings and Thermal Characteristics (T_A=25°C unless otherwise noted)

PARAMETER	SYMBOL	N-Ch LIMIT	P-Ch LIMIT	UNITS
Drain-Source Voltage	V _{DS}	30	-30	V
Gate-Source Voltage	V _{GS}	±12	±12	V
Continuous Drain Current	I _D	4.4	-3.1	A
Pulsed Drain Current (Note 4)	I _{DM}	17.6	-12.4	A
Power Dissipation	P _D	1.25		W
		Derate above 25°C		10
Operating Junction and Storage Temperature Range	T _J , T _{STG}	-55~150		°C
Typical Thermal resistance	R _{θJA}	100		100
- Junction to Ambient (Note 3)				



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N-Channel Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	30	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.4	0.72	1.2	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=4.4A$	-	37	48	mΩ
		$V_{GS}=4.5V, I_D=3.6A$	-	40	53	
		$V_{GS}=2.5V, I_D=2.5A$	-	48	66	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=30V, V_{GS}=0V$	-	-	1	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 12V, V_{DS}=0V$	-	-	±100	nA
Dynamic (Note 5)						
Total Gate Charge	Q_g	$V_{DS}=15V, I_D=4.4A,$ $V_{GS}=10V$ (Note 1,2)	-	11.3	-	nC
Gate-Source Charge	Q_{gs}		-	1	-	
Gate-Drain Charge	Q_{gd}		-	1.2	-	
Input Capacitance	C_{iss}	$V_{DS}=15V, V_{GS}=0V,$ $f=1.0\text{MHz}$	-	447	-	pF
Output Capacitance	C_{oss}		-	34	-	
Reverse Transfer Capacitance	C_{rss}		-	22	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD}=15V, I_D=4.4A,$ $V_{GS}=10V,$ $R_G=3\Omega$ (Note 1,2)	-	1.7	-	ns
Turn-On Rise Time	t_r		-	38	-	
Turn-Off Delay Time	$t_{d(off)}$		-	82	-	
Turn-Off Fall Time	t_f		-	64	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I_S	---	-	-	1.5	A
Diode Forward Voltage	V_{SD}	$I_S=1.0A, V_{GS}=0V$	-	0.77	1.2	V

NOTES :

1. Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$
2. Essentially independent of operating temperature typical characteristics.
3. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins mounted on a 1 inch FR-4 with 2oz. square pad of copper.
4. The maximum current rating is package limited.
5. Guaranteed by design, not subject to production testing



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P-Channel Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-30	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.5	-0.96	-1.3	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-3.1A$	-	82	98	m Ω
		$V_{GS}=-4.5V, I_D=-2.2A$	-	91	114	
		$V_{GS}=-2.5V, I_D=-1.1A$	-	115	165	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-30V, V_{GS}=0V$	-	-	-1	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 12V, V_{DS}=0V$	-	-	± 100	nA
Dynamic (Note 5)						
Total Gate Charge	Q_g	$V_{DS}=-15V, I_D=-3.1A,$ $V_{GS}=-10V$ (Note 1,2)	-	11	-	nC
Gate-Source Charge	Q_{gs}		-	0.85	-	
Gate-Drain Charge	Q_{gd}		-	1.4	-	
Input Capacitance	C_{iss}	$V_{DS}=-15V, V_{GS}=0V,$ $f=1.0MHz$	-	443	-	pF
Output Capacitance	C_{oss}		-	38	-	
Reverse Transfer Capacitance	C_{rss}		-	25	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD}=-15V, I_D=-3.1A,$ $V_{GS}=-10V,$ $R_G=6\Omega$ (Note 1,2)	-	2.5	-	ns
Turn-On Rise Time	t_r		-	32	-	
Turn-Off Delay Time	$t_{d(off)}$		-	161	-	
Turn-Off Fall Time	t_f		-	73	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I_S	---	-	-	-1.5	A
Diode Forward Voltage	V_{SD}	$I_S=-1.0A, V_{GS}=0V$	-	-0.79	-1.2	V

NOTES :

1. Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$
2. Essentially independent of operating temperature typical characteristics.
3. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins mounted on a 1 inch FR-4 with 2oz. square pad of copper.
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N-Channel TYPICAL CHARACTERISTIC CURVES

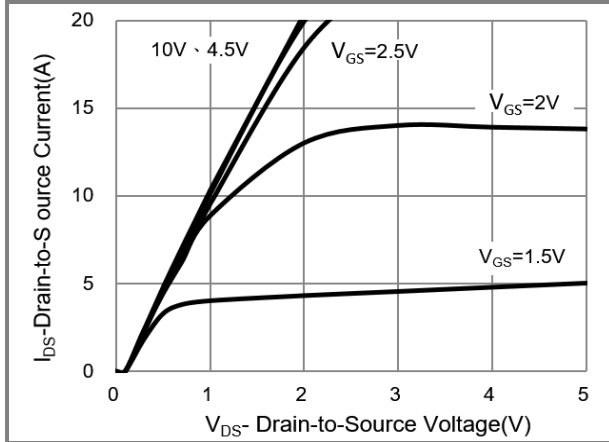


Fig.1 On-Region Characteristics

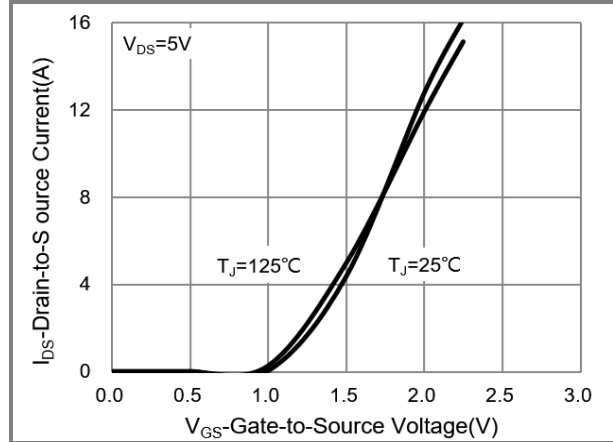


Fig.2 Transfer Characteristics

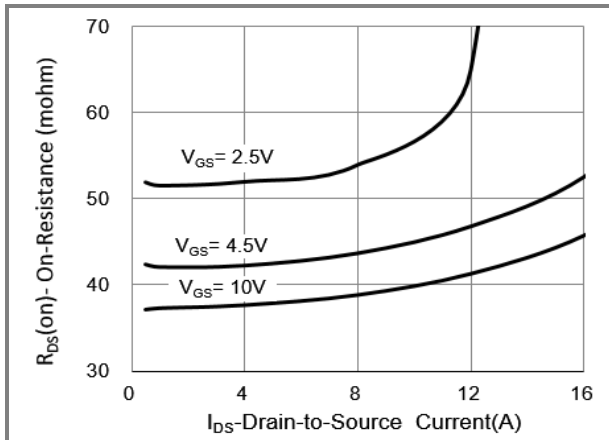


Fig.3 On-Resistance vs. Drain Current

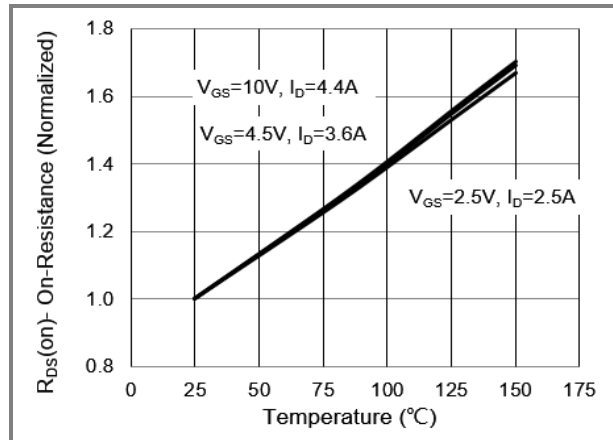


Fig.4 On-Resistance vs. Junction temperature

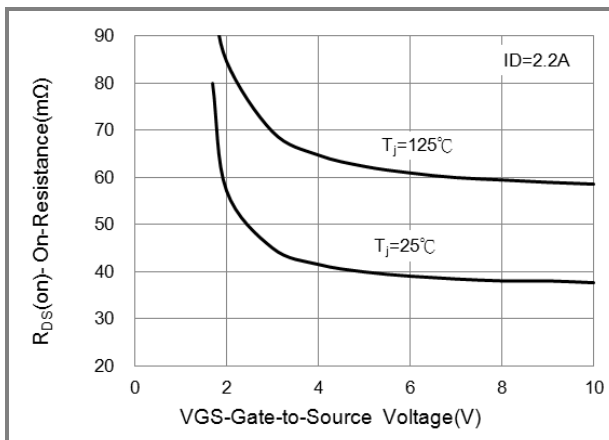


Fig.5 On-Resistance Variation with VGS.

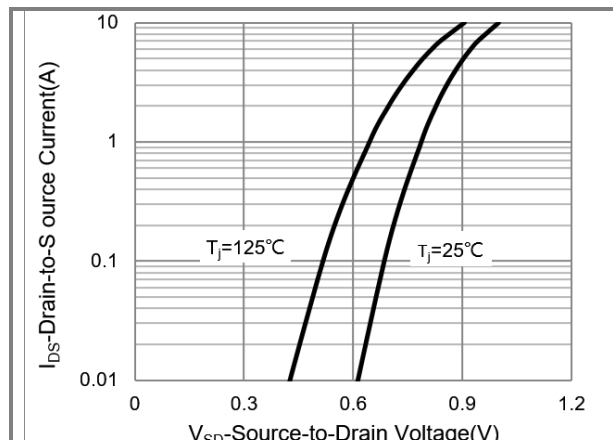


Fig.6 Body Diode Characteristics



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N-Channel TYPICAL CHARACTERISTIC CURVES

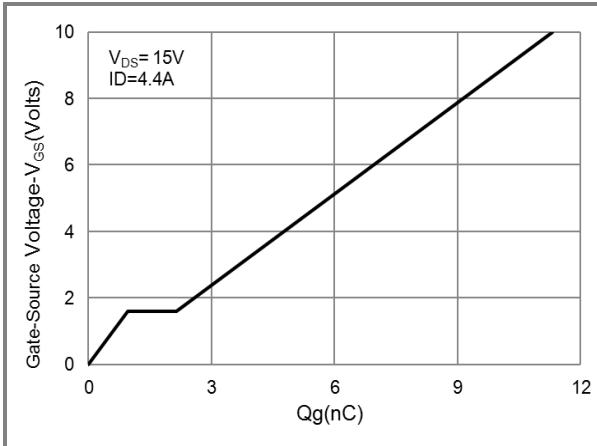


Fig.7 Gate-Charge Characteristics

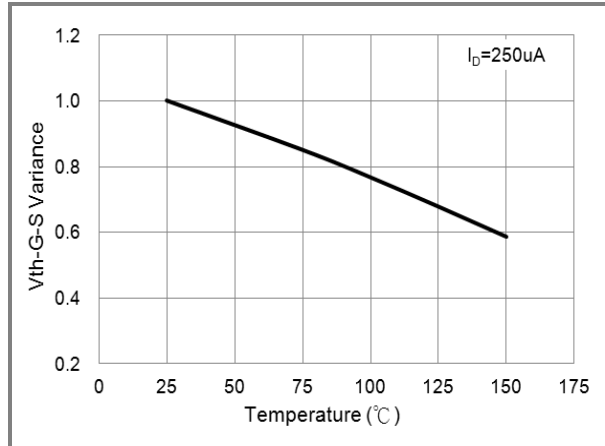


Fig.8 Threshold Voltage Variation with Temperature.

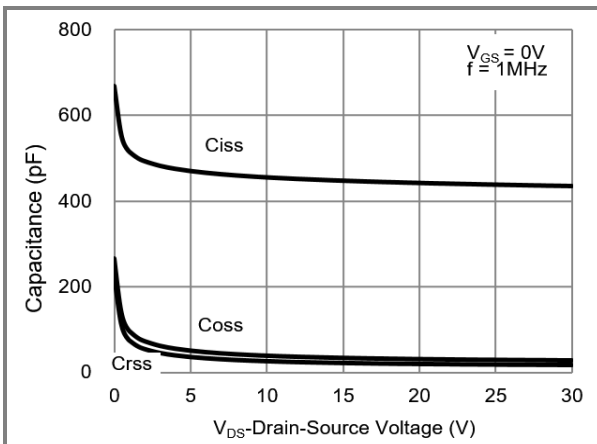


Fig.9 Capacitance vs. Drain-Source Voltage.



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P-Channel TYPICAL CHARACTERISTIC CURVES

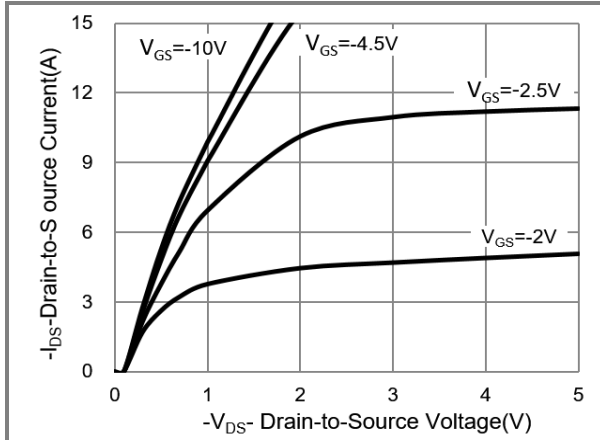


Fig.1 On-Region Characteristics

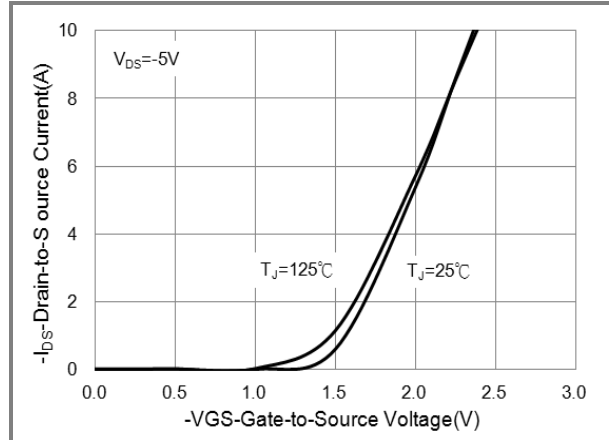


Fig.2 Transfer Characteristics

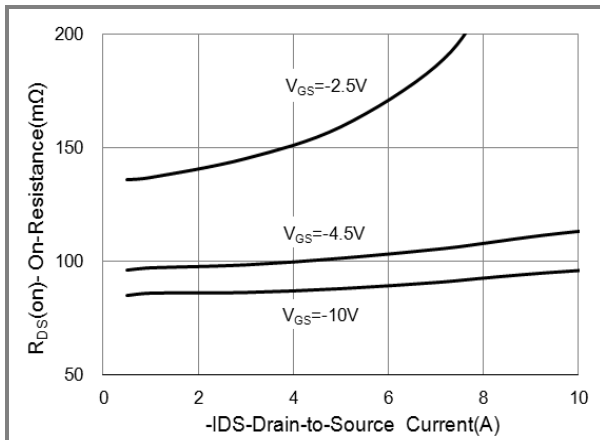


Fig.3 On-Resistance vs. Drain Current

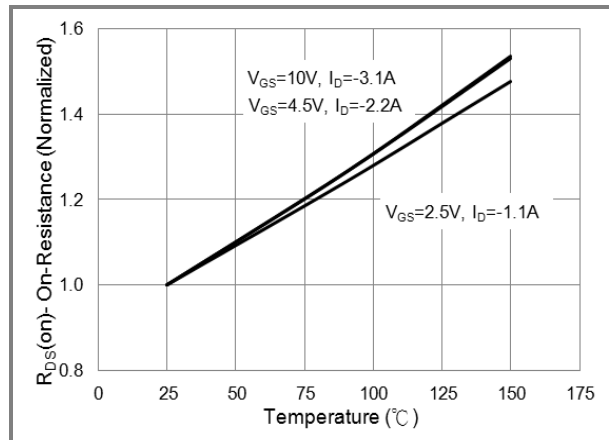


Fig.4 On-Resistance vs. Junction temperature

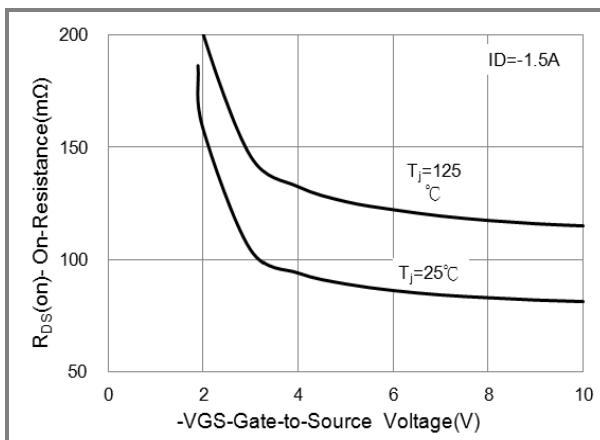


Fig.5 On-Resistance Variation with VGS.

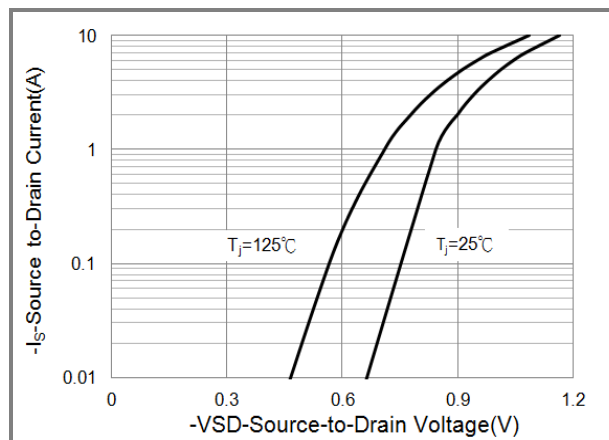


Fig.6 Body Diode Characteristics



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P-Channel TYPICAL CHARACTERISTIC CURVES

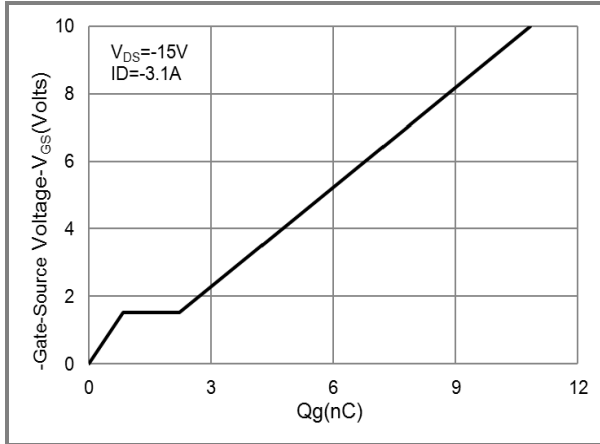


Fig.7 Gate-Charge Characteristics

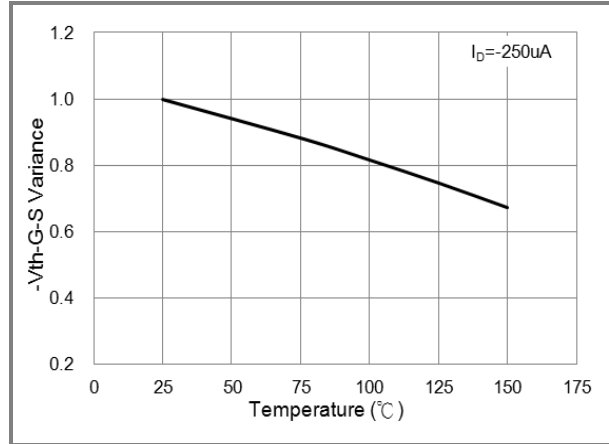


Fig.8 Threshold Voltage Variation with Temperature.

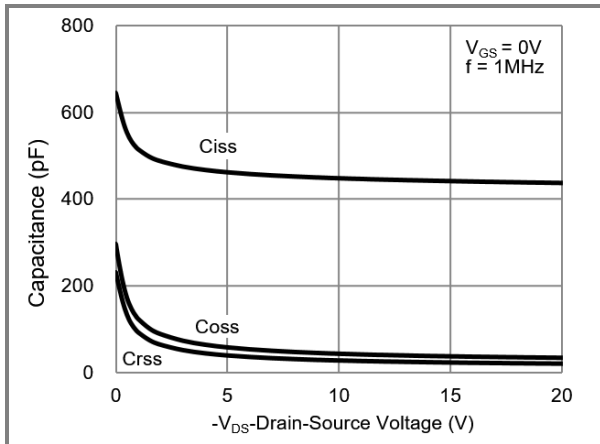


Fig.9 Threshold Voltage Variation with Temperature.

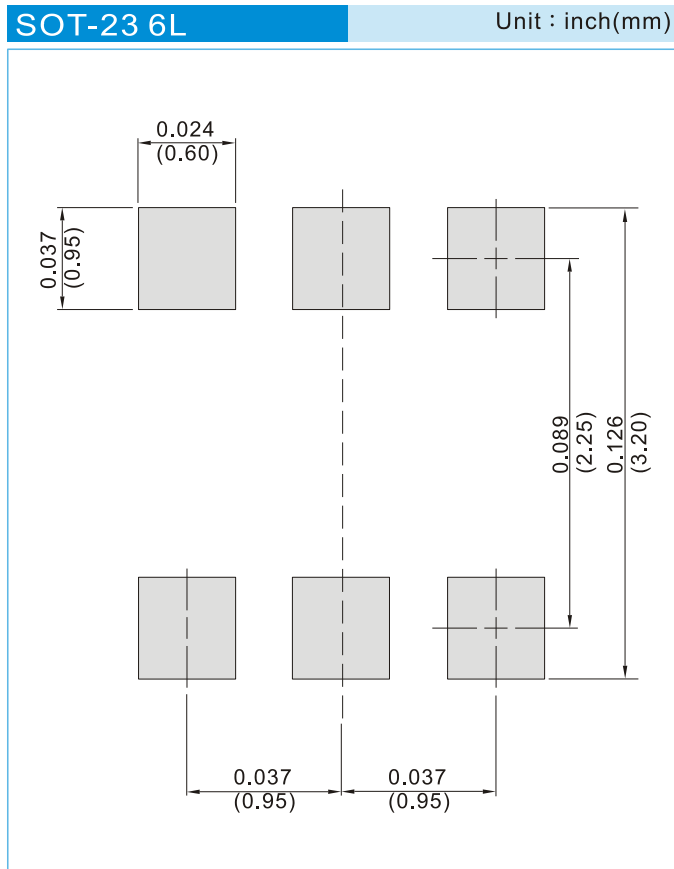


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PART NO PACKING CODE VERSION

Part No Packing Code	Package Type	Packing type	Marking	Version
PJS6604_S1_00001	SOT-23 6L	3K pcs / 7" reel	SC4	Halogen free
PJS6604_S2_00001	SOT-23 6L	10K pcs / 13" reel	SC4	Halogen free

MOUNTING PAD LAYOUT





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